Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A method for operating an integrated memory with a reduced number of external terminal pins including a ~~common external terminal pin~~ counter for internally generating addresses and ~~having~~ a memory cell field being able to be divided into a number of memory areas of uniform size, which comprises:

~~internally generating addresses with a counter of the integrated memory;~~

receiving ~~addresses and access data~~ a control signal from outside the integrated memory unit with the ~~common~~ external terminal ~~pin~~ pins;

before a memory access, partitioning the memory cell field into a plurality of memory areas, the uniform size of the memory areas or the number of the memory areas being dependent on the control signal;

for [[a]] the memory access, selecting one of the memory areas

by applying a memory area address to the external terminal pins;

for the memory access, selecting one of the memory cells inside the selected one of the memory areas by applying a memory cell address to the external terminal pins;

activating the selected one of the memory cells inside the selected one of the memory areas for a write/read access;

writing/reading data in/out of the selected one of the memory cells;

generating a further memory cell address, subsequent to the memory cell address of the memory cell on which the last write/read access was carried out, by the counter of the integrated memory for selecting a further memory cell in the selected one of the memory areas;

performing a further write/read access in the selected one of the memory areas until the further write/read access is interrupted by an interrupt command or the further memory cell address is the last memory cell address inside the selected one of the memory areas, by repeating the following steps:

activating the further selected one of the memory cells for the further write/read access;

writing/reading data in/out of the further selected one of the memory cells;

generating a further memory cell address, subsequent to the memory cell address of the memory cell on which the last write/read access was carried out, by the counter of the integrated memory for selecting a further memory cell in the selected one of the memory areas, or applying an interrupt command to the external terminal pins at a time defined by the interrupt command in order to interrupt the write/read access in the selected one of the memory areas

~~during the memory access, internally generating addresses for the access to memory cells of one of the memory areas; and~~

~~transmitting the memory area address, and, subsequently and successively, transmitting access data of the one of the memory areas through the common external terminal pin of the integrated memory~~.

Claims 2-5 (cancelled).

Claim 6 (original). The method according to claim 1, which further comprises:

applying a selection signal to the memory unit; and

transmitting at least two commands for the memory access by the application of the selection signal to the memory unit.

Claim 7 (original). The method according to claim 6, which further comprises transmitting a readout command and a write command through the selection signal.

Claim 8 (original). The method according to claim 6, which further comprises transmitting at least one of an initialization command, an interrupt command, and a masking signal through the selection signal.

Claim 9 (original). The method according to claim 7, which further comprises transmitting at least one of an initialization command, an interrupt command, and a masking signal through the selection signal.

Claim 10 (original). The method according to claim 1, which further comprises applying an activation signal to each of the

memory units for an activation of the respective memory unit given an operation of a plurality of memory units at a common data bus.

Claim 11 (original). The method according to claim 10, which further comprises additionally utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 12 (original). The method according to claim 10, which further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 13 (original). The method according to claim 1, which further comprises:

operating memory units at a common data bus; and

applying an activation signal to each of the memory units for an activation of the respective one of the memory units.

Claim 14 (original). The method according to claim 13, which further comprises additionally utilizing the activation signal

as a timing signal for operation of the respective memory unit.

Claim 15 (original). The method according to claim 13, which further comprises simultaneously utilizing the activation signal as a timing signal for operation of the respective memory unit.

Claim 16 (original). The method according to claim 1, which further comprises executing the partitioning step, the selecting step, the internally generating step, and the transmitting step only in a test mode of the memory unit for testing a functionality of the memory unit.

Claim 17 (cancelled).